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# MINILINK II - PROTOTYPE OF A MINATURE SELF-CALIBRATING FIBER OPTIC ANALOG DATA LINK

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**The purpose of the developing of a fiber optic analog data link is to make possible the monitoring of test article functioning during the exposure of that article to severe environmental conditions. The use of fiber optics to transmit the signal monitored yields immunity to electromagnetic interference (EMI) and similar potential sources of measurement interference. This report details the design and performance of a proof-of-principle prototype of such a system. The system consists of an Analog Board, a Digital Board, and a Power Assembly. The function of the Analog Board is to monitor the test point, amplify the signal with minimum frequency rolloff and distortion, and to transmit that signal via a fiber optic transmitter into an attached fiber optic cable. The Analog Board also provides for switching of both the input signal and a calibration voltage source. The function of the Digital Board is to perform automatic setting of the bias point of the fiber optic transmitter and to control the above signal switching so that automatic calibration may be achieved. The system is to be powered by batteries and is packaged in a metal enclosure**

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BLOCK 19 Abstract (Continued):

for placement in a 2.5-inch ID rocket motor section that has been emptied of propellant. The system achieved a bandwidth of dc to 4.0 MHz at a 1-volt peak-to-peak input signal and consumed 5.5 watts including a 32-percent Power Assembly efficiency.

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## I. INTRODUCTION

The purpose in the developing of a fiber optic analog data link is to make possible the monitoring of test article functioning during the exposure of that article to severe environmental conditions. In addition, the use of fiber optics to transmit the signal monitored yields immunity to electromagnetic interference (EMI) and similar potential sources of measurement interference. This report details the design and performance of a proof-of-principle prototype of such a system. To present a challenging, yet achievable goal, the instrumentation of a missile the diameter of the REDEYE was chosen. From previous work it was believed that an analog bandwidth of from DC to 5 MHz was achievable with commercial components. The system is to be powered by batteries and packaged in a metal enclosure for placement in a REDEYE motor section that has been emptied of propellant.

## II. CONSTRUCTION

The package of this prototype system (named MiniLink II) is constructed using a 1.75-inch long clip of three-inch, 3/16-inch web, aluminum angle stock. One leg is trimmed to a 1.75-inch length to form a square front panel for the module. The other leg is trimmed to 2.75 inches and it forms the base plate and mounting surface for the module. Holes are drilled and tapped into this bottom surface for mounting, and small holes are drilled and tapped into the 3/16-inch edges for attachment of a light-gauge formed aluminum cover. This aluminum chassis also serves as a heat sink for the power handling components. The layout of the front panel and the arrangement of internal circuit boards and modules can be seen in Figure 1. The front panel provides for the entrance of the signal that is being monitored via an SMA coaxial connector in the upper left corner. Also introduced via a 3 mm stereo phone jack near the lower right corner is the dc power and power control signal from the battery pack. The fiber optic connector is placed in the upper right corner. The side view of the module shows the placement of the Analog Board near the front panel, next behind that being the Digital Board, and finally after that the Power Assembly.

The Analog Board is shown in Figure 2 and the Digital Board is shown in Figure 3. The Power Assembly circuitry and a block diagram of the entire system is shown in Figure 4. The function of the Analog Board is to monitor the test point, amplify the signal with minimum frequency rolloff and distortion, and to transmit that signal via a fiber optic transmitter into an attached fiber optic cable. The Analog Board also provides for switching of both the input signal and a calibration voltage source. The function of the Digital Board is to perform automatic setting of the bias point of the fiber optic transmitter and to control the above signal switching so that automatic calibration may be achieved.

## III. ANALOG BOARD DESIGN

The analog board design as shown in Figure 2 depicts the circuitry of the signal-path section of the module. At the far left, the monitored signal is introduced via the Signal Input connector and then encounters the contacts of relay K1. There are three dry-circuit reed relays with normally-open contacts clustered between the Signal Input jack and the input to the first amplifier, U1. These relays are:

K1 - Signal Connect relay,
K2 - Input Grounding relay, and
K3 - System Calibrate relay.

After the signal passes through relay K1 contacts and amplifier U1, it is summed with a dc bias voltage at the input to U2, the second amplifier. This bias voltage (Vbias) is used to set the zero-signal current of the fiber optic transmitter (X1) to the center of the linear portion of its current-to-photon transfer characteristic. The network of Q1, X1, R7, and C2 provide for current gain and degenerative feedback so that X1 is properly driven with signal and the bandwidth is preserved. The resistors R5 and R6 are current limiting load resistors, with R6 serving as a current monitoring resistor for X1. Also shown are the relay coils and their spike suppression circuitry. Several voltages and currents are shown entering and exiting the Analog Board these are:

GND, -12V, +12V: Ground and circuit power input from the Power Assembly.
Vcal: Calibration Voltage; a voltage reference input which is generated on the Digital Board and is used for system calibration.
Vbias: Bias Voltage; a voltage input, also generated on the Digital Board, used for setting the operating current of the fiber optic transmitter, X1.
Vtp1: Test Point 1 Voltage; voltage generated by resistor R6 which is proportional to bias current flowing through X1.
VK1, VK2, VK3: Voltages supplied from the Digial Board which activate the coils of K1, K2, and K3.

## IV. DIGITAL BOARD DESIGN

The Digital Board is shown in Figure 3. The purpose of this board is to provide the sequencing of events and the various voltages required to elicit proper operation from the Analog Board. The basic concept of the MiniLink II module is that at initial power-on or at any subsequent cycling off-on of power, the module will perform a self-setting and calibrate function before the monitored signal is transmitted. The desired sequence of events is as follows:

0 - Power-On
1 - Reset Cycle - Clear the counter of Ramp Voltage Generator (U4) to initial state (Vbias = zero volts).
2 - Pull in (close) contact of K2 so that input to the first amplifier (U1) on the Analog Board is at zero signal.
3 - Generate a voltage for Vbias which increases ramp-fashion so that the fiber optic transmitter X1 is given an increasing current with respect to time.
4 - When the X1 bias current is properly set, (as indicated by the voltage Vtp1) terminate the voltage ramp and hold that value steady until the next power off-on cycle.
5 - Drop out (open) contact of K2 to unground the input of U1 on the Analog Board
6 - Pull in contact of K3 to transmit the calibration voltage Vcal through the analog system for approximately 2 seconds so that scale setting may be accomplished.
7 - Drop out K3, delay for approximately 2 seconds to provide a zero-signal reference.
8 - Pick up K1 to connect monitor point signal to the input of the analog system.
9 - Monitor the average value of the current through X1. If it exceeds a safe level, perform a Reset cycle from step 1 in an attempt to prevent damage to X1. This may result in a continual recycling of Reset which would indicate circuit failure or an overdriving signal from the monitor point.

In order to accomplish the above, an assembly of voltage comparators and a binary counter is used. One section of a quad comparator (U3d) is wired to be a relaxation oscillator and generates a train of rectangular pulses. This signal is fed to the 8-bit synchronous binary counter U4 which, if not limited by outside signals, would continually count in cycles from zero to 255. A second cell of the comparator (U3a) forms the Clear One-Shot circuit. This circuit detects the power-on sequence and causes the counter U4 to be cleared to zero. Subsequently, Clock pulses are received and the count on U4 advances by binary values. The resistors R17 through R24 have resistance values which are weighted by the binary sequence (1, 2, 4, 8, etc.) so that binary weighted elements of current are summed at the output terminal Vbias. As the count on U4 advances, a linearly-rising voltage ramp appears at this point and is provided to the Analog Board for X1 bias setting. A third cell of the comparator (U3c, Bias Comparator) monitors the voltage value of Vtp1 (which is proportional to the X1 bias current) and when it exceeds the reference voltage as set by R27, it will halt the advancing of the count on U4 and retain the Vbias voltage value attained.

Comparator cell U3c also sends a signal to U5b which is a cell of a high-current voltage comparator that is used to drive the coil of relay K2, the Input Grounding relay. This signal causes U5b to cease providing current to K2. The network C15, R43, and C16 provide a signal at the input to cell U5c which causes the System Calibrate relay, K3, to be activated for about two seconds. When the voltage on the inverting input of U5c drops below the voltage at its noninverting input, this cell ceases to drive K3 and the application of Vcal to the analog system is discontinued. The attendant rise of voltage at the output of U5c reverse-biases diode CR8 which, to this time, has been preventing capacitor C14 from being charged. C14 now is charged through R41 and when that voltge exceeds the voltage across R40, cell U5a will provide current to relay K1 which will connect the input signal from the monitor point to the analog system.

The comparator cell U3b (Limit Comparator) serves as a "watchdog" of the average current through the fiber optic transmitter, X1. It monitors Vtp1 and compares against the voltage developed across series resistors R26 and R27. This level is set to correlate to the maximum safe current through X1. When an excessive current is detected, the output of U3b is coupled via C12 into the Clear One-Shot (U3a) and via U5d to the Bias Comparator (U3c), thus, initiating a Reset cycle. This procedure will relieve the X1 over-current for a time and provide an obvious signal to the user of the system that an overload condition exists.

## V. POWER ASSEMBLY

The Power Assembly uses a combination of discrete, integrated, and modular components to achieve the power switching, conditioning, and regulation required by the analog and digital boards. DC power and the Power Control signal are brought into the MiniLink II module via a three-contact phone plug. The dc is supplied from a battery pack or missile system power of between 15 volts and 30 volts. The Power Control signal is a voltage which, when near the value of the dc input, will cause the MiniLink II module to begin functioning. For this prototype, the Power Control signal is generated by an air-pressure switch. Referring to Figure 4, the Power Control signal is fed to the base of transistor Q2 which turns on and supplies current to the positive 12-volt regulator U6, the voltage inversion module U7, and the positive 5-volt regulator U8. This transistor switching circuitry is made necessary because the only air-pressure switches readily available at the time of this prototype had only a few milliamps of contact current rating.

## VI. TESTING

Figure 5 shows frequency response curves for two examples of the Analog Board, the "Preliminary" and the "Packaged" versions. These examples differ only in the more cramped geometry of the Packaged version which includes the relay circuitry at the input of U1. These curves were taken using a one-volt peak-to-peak sine wave from a Tektronix FG-504 generator applied to the Signal Input connector. The signal was transmited via a 20-foot length of optic fiber to a Math Associates RA-1000 analog receiver module and monitored on a Tektronix 7834 oscilloscope. In both cases, the frequency response is flat within plus or minus 0.2 decibel from dc to 1.0 MHz, and falls below 3.0 decibels at 4.0 MHz for the Packaged unit and 4.5 MHz for the Preliminary unit. Although this is not quite the originally-desired bandwidth, this is quite useful for most missile system network monitoring purposes.

Testing of the sequencing of the automatic calibration system is shown in the scope photos of Figure 6. The upper three traces in the photo "Early-Time Functions" shows voltages from the three relay comparator/coil drivers (U5a through U5c on the Digital Board). The trace, if it is near the baseline, indicates that the coil is energized and the relay contacts are closed. The bottom trace is the output of the RA-1000 fiber optic receiver which is monitoring the output of the fiber optic transmitter. All traces start with the power being switched on at the left of the photo. After about 14 milliseconds, the Reset sequence is finished and the traces indicate the intended states of relays K1 and K3 being open and K2 being closed. This provides a zero-input state for accurate setting of the X1 bias which starts immediately as indicated by the ramp voltage shown by the trace "F/O Out." At about 33 milliseconds into the sweep this rising voltage suddenly flattens out and holds at the maximum level atained and relays K2 and K3 change states. This indicates that the Bias Comparator (U3c) on the Digital Board has detected the proper bias current for X1 and has halted its increase. At this state, U5b causes K2 to de-energize and unground the input to the analog amplifier chain. Once this is accomplished, U5c (the comparator/driver for K3) pulls in K3 which applies the calibration voltage to the input of the analog amplifier circuitry.

The photo "Late-Time Functions" extends the above sequence with a slower sweep time to show operations up through the start of the transmission of analog signal. Starting near the left of the photo, all of the traces continue at the final state observed in the first photo until about 2.0 seconds into the sweep. At this point relay K3 is de-energized removing the calibration voltage from the input to the analog amplifier. This can be observed in the bottom trace "F/O Out" as a small drop in the observed output. At a later time, about 7.2 seconds into the trace, relay K1 is energized by U5a which connects the monitored signal (here a 1.0 KHz sine wave) into the analog amplifier. This transition can also be seen in the "F/O Out" trace in the last second of sweep.

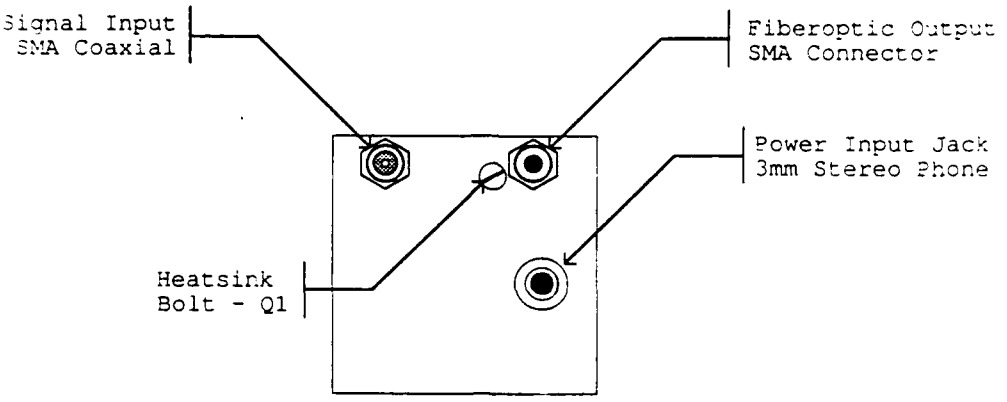
The power consumption of this system is rather modest considering its complexity and functionality. The current drain from the various voltage supplies is as follows:

Positive 12 volts; 98.38 milliamps
Negative 12 volts; 26.07 milliamps
Positive 5 volts; 41.35 milliamps.

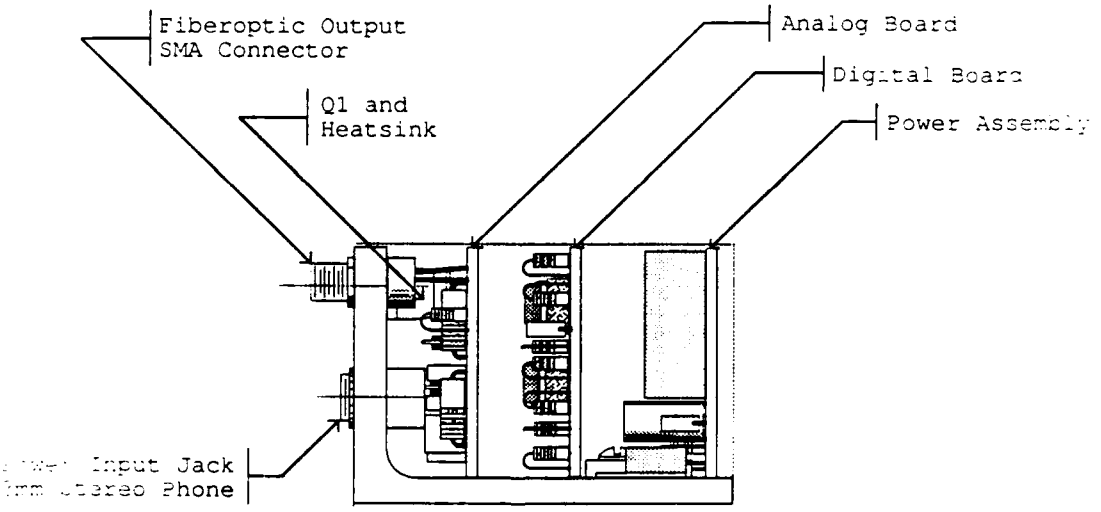
This yields a power consumption of 1.70 watts for the Analog Board and the Digital Board. The total power input to the module at 15 volts is 358.2 milliamps. This yields a power requirement of 5.37 watts and indicates a Power Assembly conversion efficiency of about 32 percent. At present, the Power Assembly is made up of two linear regulators for the positive voltages and a switching module for the negative voltage. This efficiency is to be expected with that technology. Higher efficiencies can be obtained with fully-switching converter designs and subsequent improvements in this design will feature same. Since power on/off control is inherent in the design of MiniLink II, this efficiency should present little problem for most envisioned uses.

## VII. CONCLUSIONS

The telemetry system described herein is shown to be fully functional in self adjustment and calibration as intended and is of frequency response sufficient for most missile network monitoring applications. In addition, it is of compact size, reasonably low power consumption and self protecting in case of accidental overload at the input. Since this system uses readily-available commercial parts, it is easily duplicated so that it, or custom variations of it, can be constructed for any specific application.




MiniLink II - Front View




MiniLink II - Side View

**Figure One. MiniLink II Module Layout.**

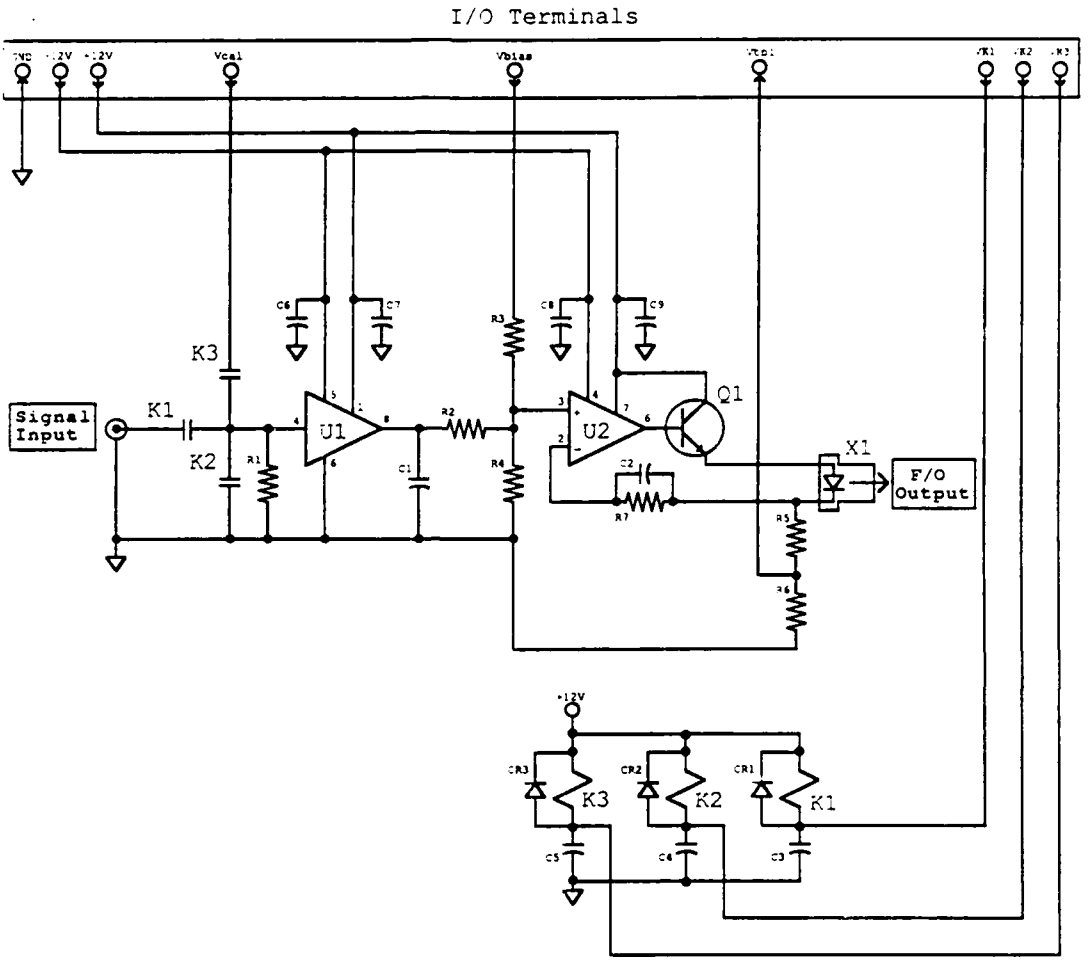



**Figure Two. MiniLink II Analog Board.**

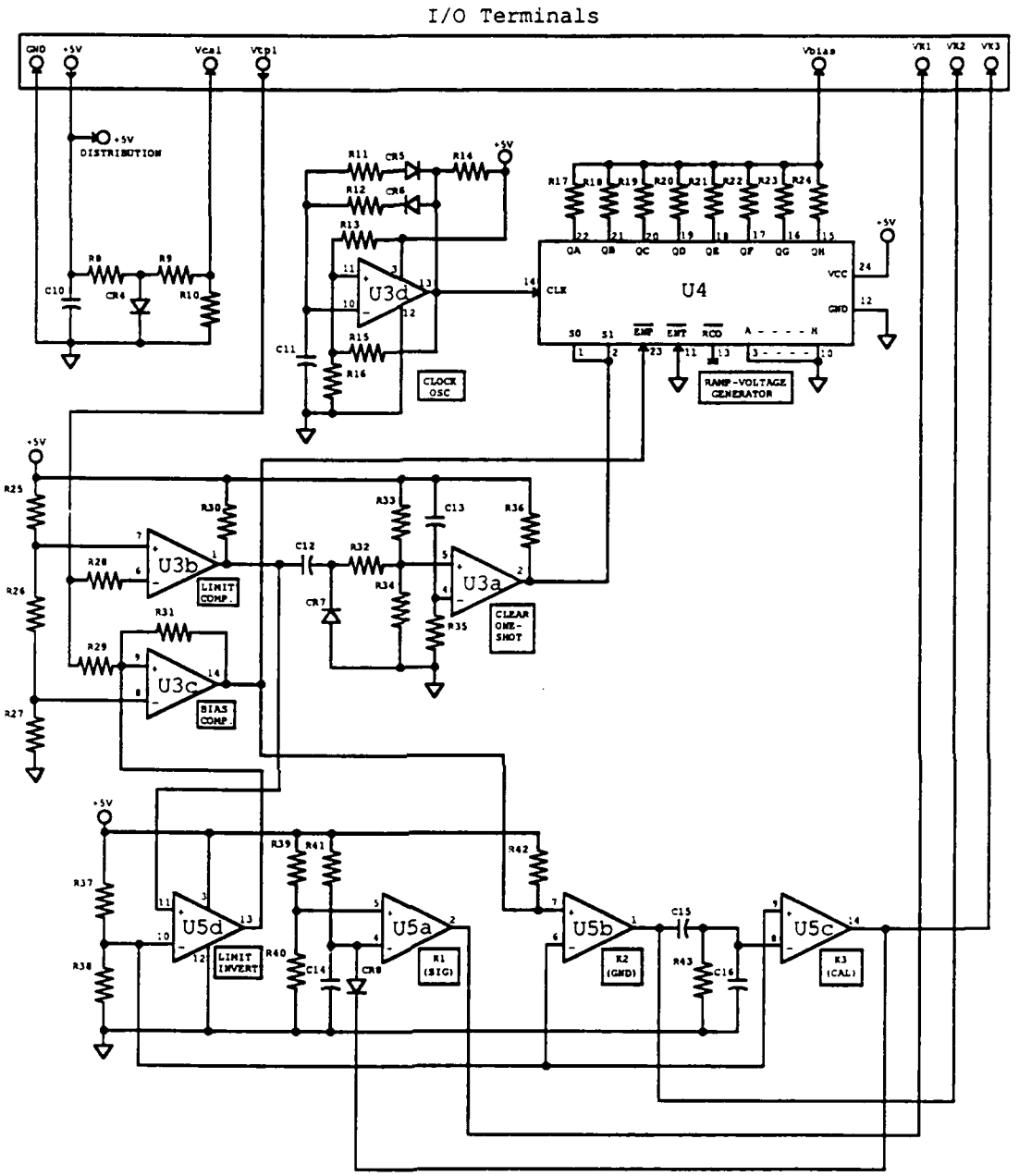



**Figure Three. MiniLink II Digital Board.**

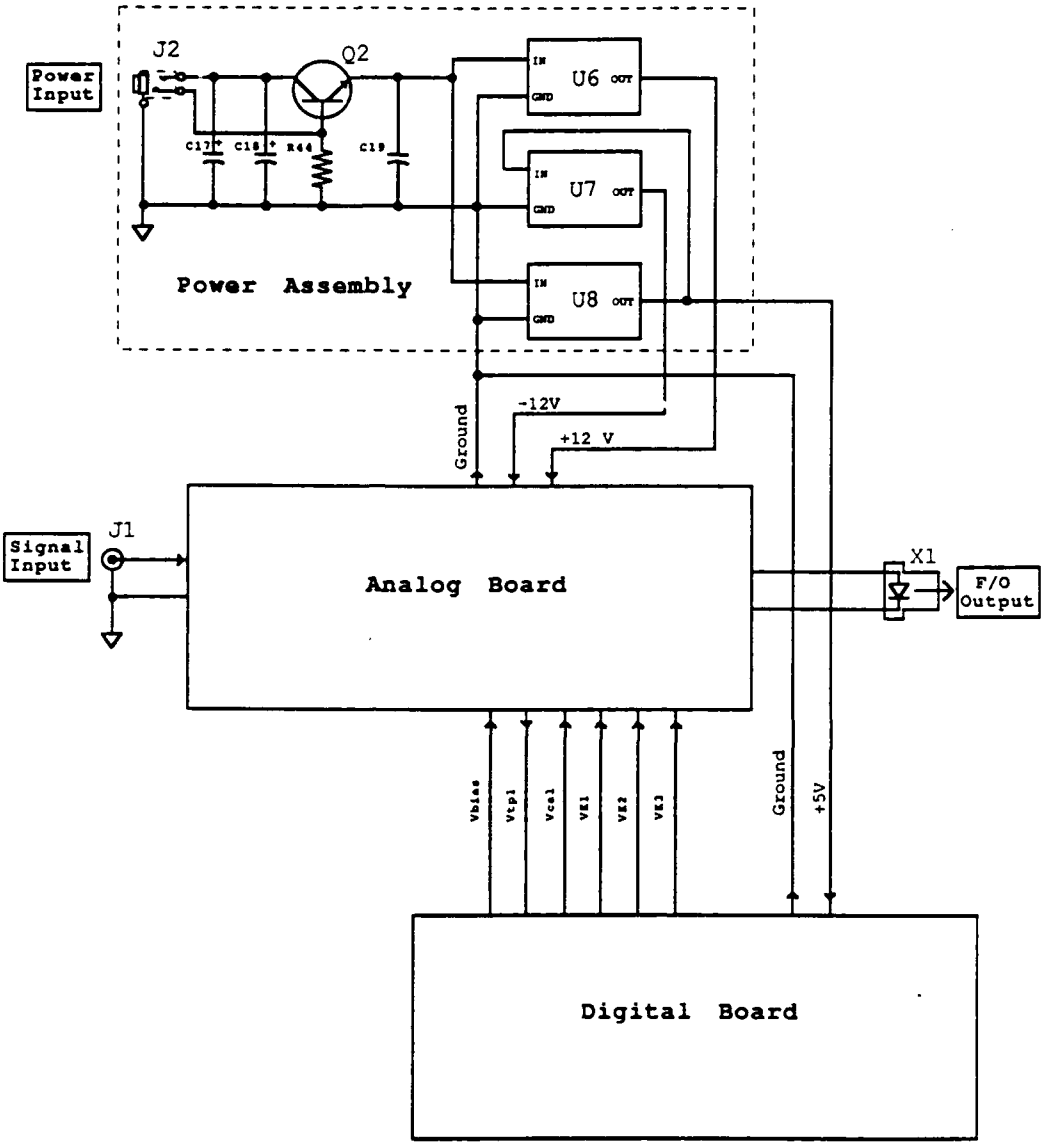



**Figure Four. MiniLink II Power Assembly.**

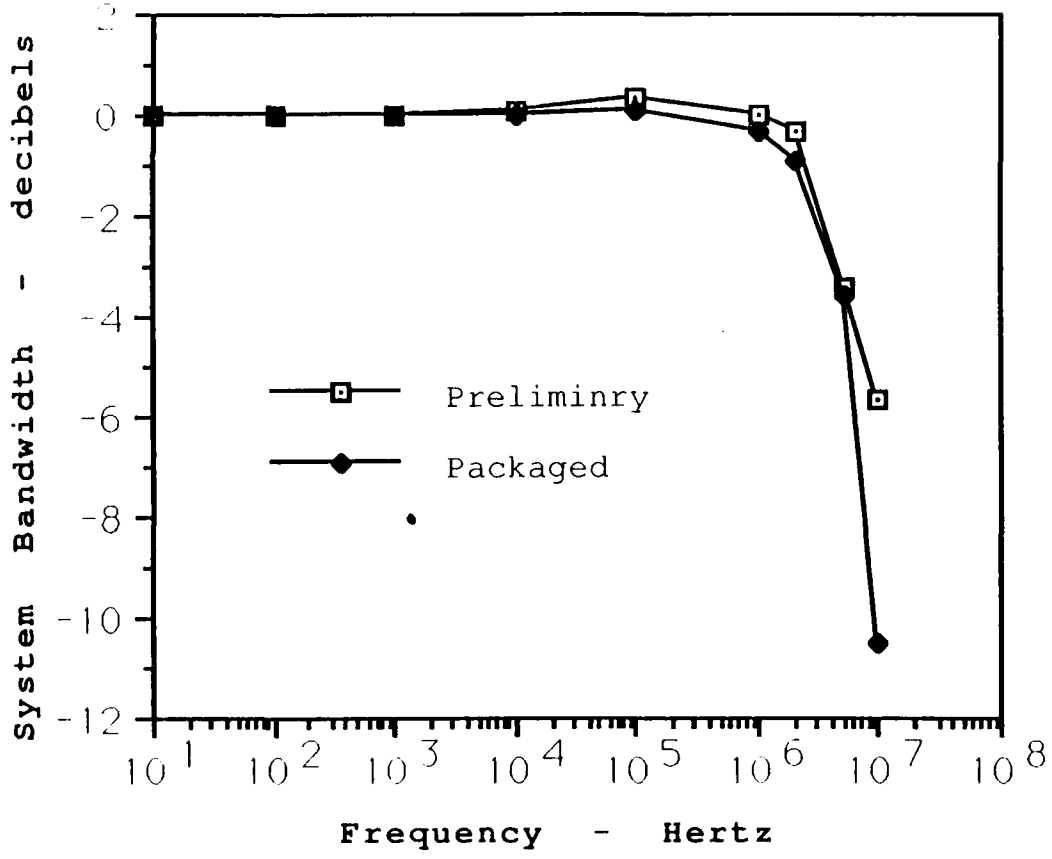
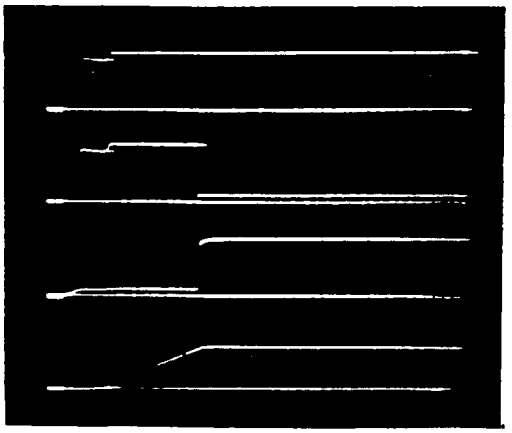
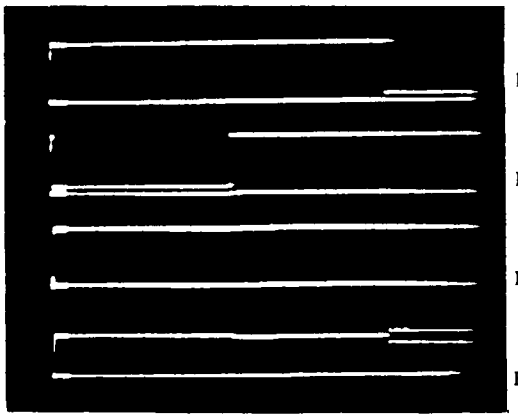



Figure Five. MiniLink II - Bandwidth.




Horizontal = 10 mS/cm : Vertical; K1, K2, K3 = 10 volts/cm, F/O Out = 5 volts/cm

Early - Time Functions




Horizontal = 0.5 S/cm : Vertical; K1, K2, K3 = 10 volts/cm, F/O Out = 5 volts/cm

Late - Time Functions

Figure Six. MiniLink II - Module Sequencing.

# APPENDIX

## COMPONENT TYPES AND VALUES

# COMPONENT TYPES AND VALUES

## Resistors

All resistors are 5%, 1/4 watt, carbon composition type unless otherwise noted.

R1, R31 = 3.3 K
R2, R3, R21, R28, R29 = 1.0 K
R4, R32, R36 = 10 K
R5 = 39 ohm, 1/2 watt
R6 = 10 ohm, 1/2 watt
R7 = 4.7 K
R8 = 560 ohm
R9, R10, R44 = 12 K
R11, R13, R15, R16, R33, R34, R35 = 1 Meg
R12 = 100 K
R14, R17 = 15 K
R18, R40 = 8.2 K
R19 = 3.9K
R20 = 1.8 K
R22 = 470 ohm
R23 = 220 ohm
R24 = 100 ohm
R25, R30 = 2.2 K
R26 = 330 ohm
R27 = 270 ohm
R37 = 100 K
R38 = 47 K
R39 = 2.2 K
R41, R43 = 680 K
R42 = 6.8 K

## Capacitors

All capacitors are ceramic MIL-C-39014 types unless otherwise noted.

C1 = 330 picofarad
C2 = 6 picofarad
C3 through C9 = 1 microfarad
C10, C13, C15, C16 = 1.0 Microfarad
C11, C12 = 100 picofarad
C14 = 2.0 microfarad
C17, C18 = 1.2 microfarad, 35 volt tantalum
C19 = 0.1 microfarad

## Semiconductors and Relays

U1 = HA5033: Harris wideband buffer amplifier
U2 = LM318: wideband operational amplifier
U3 = LM339: Quad voltage comparator
U4 = 74ALS867: 8-bit synchronous binary counter
U5 = CMP404: PMI high current voltage comparator
Q1 = 2N3053: silicon NPN transistor
Q2 = MJE1100: silicon NPN Darlington transistor
CR1 through CR3 = 1N4001: silicon rectifier
CR4 through CR8 = 1N4148: silicon switching diode
X1 = HBFR-1204: HP 820 nm fiberoptic transmitter
K1 through K3 = JWS-117-3: P&B SIP dry circuit reed relay

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